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TITLE: Multiplex ATM/STM converter for structured data

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INVENTOR-INFORMATION:

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US-CL-CURRENT: 370/395.6, 370/409 , 370/517

ABSTRACT:

The disclosed device allows de-ceiling of ATM cells in structured data transmission according to ITU-Telecommunication Recommendation I. 363, reproduction of a plurality of STM frames represented at a speed of 64 kbps.times.n (n=any natural number), and moreover, discloses an architecture that allows a minimum of the buffer amount due to the de-ceiling. The ATM/STM converter according to the present invention includes an AAL1 processor 101, a common buffer section 102 that stores ATM cell payloads using link-list queues and in which a pointer within that link list is also stored, a write controller 103 that manages write addresses to the common buffer section, a read controller 105 that manages read addresses to the common buffer section, an empty cell address FIFO section 104 that manages a list of empty cell addresses within the common buffer section, a buffer initialization controller 107 that initializes the common buffer section, a frame position detector 108 that monitors the frame position of STM signals, and a CM section 106 that relates channel arrangement on the STM side with VP on the ATM side.

7 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

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Detailed Description Text - DETX (5):

Upon receiving notification of the arrival of new cells and their VP numbers from AAL1 processor 101, write controller 103 selects the VP register value S103 from a tail register value recorded in VP units (Channel units on the STM network side) held within write controller 103 and forwards that register value as the cell block address of that VP to common buffer section 102. Further, in relation to that VP, write controller 103 receives the cell block address S104 of the next inputted ATM cell from empty cell block address FIFO section 104, and updates the value of the tail register of that VP within write controller 103. At the same time, write controller 103 also forwards this new cell block address written to the tail register to common buffer section 102, and notifies buffer initialization controller 107 that writing of ATM cells has occurred.

tion controller 107, and frame position detector 108, and inputs ATM cell S101 to AAL1 processor 101.

Upon inputting ATM cell S101, AAL1 processor 101 executes SAR/CS layer processing, and as one result of this processing, extracts the frame positions of STM frames. AAL1 processor 101 also adds to the user data a frame position designation bit that indicates whether a frame or not, a buffer initialization request bit from buffer initialization controller 107, and a P-format bit that indicates whether ATM cells, which are data stored in a cell block, are P format or non-P format, and transmits the user data to common buffer section 102. FIG. 6 shows the data format of signal S102 that is inputted to common buffer section 102. AAL1 processor 101 also recognizes the VPI of inputted cells (virtual path identifier), and signals the VPI to the write controller 103.

Common buffer section 102 contains cell buffer section 202 as will be described hereinbelow, the cell buffer section 202 having queues in VP units (channel units on the STM network side), and each of the queue blocks store a payload of a respective ATM cell. These blocks will hereinafter be referred to as "cell blocks." Each address within the cell buffer section 202 is pointed by two types of addresses, a cell block address designating a cell block and an offset address which is the offset within each cell block. Common buffer section 102 receives ATM cells having the format of FIG. 6 from AAL1 processor 101, and these ATM cells are written to the common buffer section 102 in VP units to cell block addresses signaled from write controller 103. Common buffer section 102 also receives cell block address S104 from write controller 103 for the next inputted cells and holds S104 as data. Details regarding the construction and operation of common buffer section 102 will be described hereinbelow with reference to FIG. 3.

Upon receiving notification of the arrival of new cells and their VP numbers from AAL1 processor 101, write controller 103 selects the VP register value S103 from a tail register value recorded in VP units (Channel units on the STM network side) held within write controller 103 and forwards that register value as the cell block address of that VP to common buffer section 102. Further, in relation to that VP, write controller 103 receives the cell block address S104 of the next inputted ATM cell from empty cell block address FIFO section 104, and updates the value of the tail register of that VP within write controller 103. At the same time, write controller 103 also forwards this new cell block address written to the tail register to common buffer section 102, and notifies buffer initialization controller 107 that writing of ATM cells has occurred.

Frame position detector 108 monitors the ON/OFF of the frame position designation bit in data S110 read out from common buffer section 102 (FIG. 6), and when ON, signals the instructions to read controller 105 (S111). CM section 106, according to timing of the STM network side, signals the VP to be read out to read controller 105 and buffer initialization controller 107.

Based on frame position (S111) signaled from frame position detector 108, read controller 105 reads the VP designated by CM section 106 and synchronized with the timing of the STM network side. In addition, read controller 105 notifies the cell block address of a VP for which read-out is completed as an empty cell address to empty cell address FIFO section 104 and buffer initialization controller 107. A detailed description of the construction and operation of read controller 105 will be presented hereinbelow with reference to FIG. 3.

Buffer initialization processor 107 receives VP number S114 from CM section 106, information S103 indicating that writing has occurred for each VP unit from write controller 103, and also receives as S112 from read controller 105 information indicating that read-out has occurred for each VP unit, and calculates the queue length of each VP unit in the cell buffer section by a method to be explained hereinbelow. From the results of this calculation, buffer initialization controller 107 performs comparison on three points: (1) that the queue is empty (2) that the queue is 2n times the frame length (n being the CDV value within the network divided by 125 μ sec), (3) that the queue is n times the frame length, converts the results to signals (S201, S203) for use by buffer initialization control, and signals write controller 103 and read controller 105. Details regarding the construction and operation of buffer initialization controller 107 will be described hereinbelow with reference to FIG. 4.

Empty cell address FIFO section 104 manages empty cell block addresses in common buffer section 102 within empty cell address FIFO section 104, signals empty cell block addresses S104 stored at the head of empty cell address FIFO 104 in response to requests from write controller 103, and when read controller 105 completes read-out of a VP, stores that cell block address S112 at the end of empty cell address FIFO as a newly empty cell block address.

FIG. 3 is a block diagram showing the detailed construction of common buffer section 102 shown in FIG. 2. The common buffer section 102 is provided with cell buffer section 202, pointer buffer section 201, latch section 204, and counter 203. Cell buffer section 202 includes queues in VP units (channel units on the STM network side), and individual blocks of the queues store payloads of individual ATM cells and individual blocks of the queue are pointed out by two types of addresses: addresses in cell block units and offset addresses within individual cell blocks. Pointer buffer section 201 stores queue pointers (cell block addresses) of a link list structure in cell buffer section 202. Latch section 204 latches addresses (cell block addresses) in cell block units. Counter 203 carries out a count to 46 or a count to 47 depending on whether inputted ATM cells are P format or non-P format, respectively.

The common buffer section 102 of this embodiment functions as follows. Common buffer section 102 receives data having the format of FIG. 6 from AAL1 processor 101, and transmits cell block addresses and inputted cells to cell buffer section 202 to write to cell block addresses signaled from write controller 103. From the P-format bit of input data S102 shown in the format of FIG. 6, counter 203 receives notification of whether the inputted cells are P format or non-P format and counts up from 0 to 46 or 47, respectively. Cell buffer section 202 recognizes cell block address S103 signaled from write controller 103 and offset address S105 received from counter 203 as the stored address of an inputted cell, and writes the payload portion of the inputted cell to its internal memory. Latch section 204 latches the cell block address to which the inputted cell is written. Pointer buffer section 201 receives from write controller 103 cell block address S104 for the inputted cell following that VP, and writes S104 as data, in internal memory using the cell block address S103 latched by latch section 204 as the address in the internal memory.

FIG. 7 shows the link list management structure of VP units in common buffer section 102. Here, a link list is shown by which the payload of an ATM cell and a pointer designating the position of storing the next ATM cell, respectively, are stored in the addresses of cell buffer section 202 and pointer buffer section 201 designated by the same